REMARKS

Claims 1-4 are the claims that have been examined in the current application. Claims 1 and 3 are objected to as lacking an antecedent basis for the limitation "the permissible temperature" in the last paragraph of the respective claims. Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Schmook et al. (6,624,994) in view of Taki et al. (US 6,474,762).

Preliminary Matters

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority under 35 U.S.C. § 119, as well as receipt of the certified copies of the priority documents.

Applicant also thanks the Examiner for acknowledging acceptance of the drawings filed December 29, 2004.

Further, Applicant thanks the Examiner for considering and initialing the Information Disclosure Sheet also filed December 29, 2004.

Claim Objections

1. Claims 1 and 3 are objected to as lacking an antecedent basis for the limitation "the permissible temperature" in the last paragraph of the respective claims.

By this Amendment, Applicant has amended claims 1 and 3 to cure the Examiner's objection. Applicant respectfully requests the Examiner withdraw the stated objection.

§103(a) Rejection

2. Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Schmook et al. (6,624,994) in view of Taki et al. (US 6,474,762). Applicant respectfully traverses.

Claims 1 and 3 recite "setting a constant of the circuit element so that the reference voltage is not greater than a critical voltage, wherein the critical voltage is a product of an on-resistance of the semiconductor device when its channel temperature is at an upper limit of the permissible temperature, and a minimum current value which causes the channel temperature to reach the upper limit of the permissible temperature by the self-heating due to Joule heat." The Examiner acknowledges that Schmoock fails to teach this element of the claimed invention, but argues that Taki teaches the limitation. The Examiner cites to column 10, lines 37-48, along with FIG. 9 of Taki as teaching the limitation. Applicant respectfully disagrees. FIG. 9 of Taki teaches an amplifier circuit with a thermistor to prevent thermal runaway of the transistors. To do so, Taki connects a thermistor in parallel in order to by-pass the resistor 25, which reduces voltage between the base-emitter of the transistors when the voltage rises due to self-generation of heat. The thermistor is chosen because it has the same resistance value as the resistors, not because it prevents a critical voltage from being reached. Further, Taki fails to teach that the critical voltage in question is a product of an on-resistance of the semi-conductor and a minimum current value.

In more detail, when the FET is used in an ohmic region according to the present invention (i.e. when a drain-source voltage is dropped by applying a fully voltage between a gate and a source of the FET and an on-resistance is saturated around 10m Ω), the critical voltage is defined as a product of an on-resistance of the FET when its channel temperature is at an upper limit of the permissible temperature, and a minimum current value of a drain current which causes the channel temperature to reach the upper limit of the permissible temperature. The overcurrent determining value is set to a value that is smaller than the critical voltage. When the

drain-source voltage exceeds the overcurrent determining value, it is determined as the overcurrent, and proceeds to a protection operation.

On the other hand, Taki fails to show a concept of the on-resistance. A load current control transistor of Taki is Q5 and Q6. Q5 and Q6 are operated as a class amplifier. Q5 and Q6 are arranged as an emitter follower, and a large voltage potential difference occurs between the emitter and the collector. That is, Taki does not show an operation when the voltage difference between the collector and the emitter is saturated. Therefore, Q5 and Q6 of Taki are operated regardless of the concept of the on-resistance recited in the present invention.

Further, even if the voltage difference between the collector and the emitter is saturated, a collector current, Ic, is dependent on a base current, Ib, since Q5 and Q6 are Bipolar Transistors (NPN, PNP). Then, a current amplification factor represents β. In this case, Ic is represented as following formula. $Ic = \beta * Ib$

As shown in the above formula, the concept of on-resistance is not derived from the above formula. Certainly, the critical voltage is not derived from the above formula.

Additionally, the Examiner asserts that "Taki at al, further teaches that the voltage 0.5V is a product of an on-resistance 16.2 ohms of the semiconductor devices Q5 and Q6 and a minimum current Value 30 mA as disclosed in Col. 10, line 37-48 and Fig. 9." in page 3, the second full paragraph in the Office Action. However, the applicant believes that "16.20 Ω" of Taki is merely a resistance value of resistance 25, and is not the on-resistance of the semiconductor devices Q5 and Q6. Further, a current having "a minimum current Value 30 mA" of Taki is not flowed in the semiconductor devices Q5 and Q6. The current having "a minimum current Value 30 mA" is flowed in the semiconductor devices Q3 and Q4. Furthermore, "the

voltage 0.5V" of Taki merely indicates a voltage drop of the resistor 25. The voltage drop of the resistor 25 is not relevant to the voltage drop of the present invention that occurs by flowing a load current to the semiconductor.

Moreover, in Taki, the thermistor detects a rise in temperature of Q5 and Q6. When the temperature of Q5 and Q6 is raised, a current flowing in Q5 and Q6 is controlled so as to be decreased. That is, the temperature of Q5 and Q6 is indirectly detected by using the thermistor 26 in Taki.

On the other hand, in the present invention, the channel temperature is directly detected and controlled by using a property that the channel temperature of FET to be protected against overheat linearly correlates with the on-resistance. The property that the channel temperature of FET linearly correlates with the onresistance leads to the concept of the critical voltage, further, the present invention achieves to control the channel temperature so as not to exceed the upper limit of the permissible temperature even if any load current such as the overcurrent flows into the FET by setting the overcurrent determining value to a value that is smaller than the critical voltage.

Thus, the references fail to disclose all of the limitation of claims 1 and 3, and claims 1 and 3 are patentable over the applied art. Claims 2 and 4, by virtue of their dependencies from claims 1 and 3, respectively, are also patentable over the applied art.

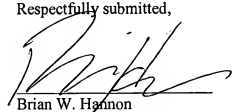
Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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